CLAIMS

What is claimed is:

1. An amplifier comprising:
   a. a power terminal;
   b. a load transistor having a first load terminal connected to the power terminal, a second load terminal, and a load-control terminal;
   c. an input transistor having a first current-handling terminal connected to the second load terminal, a second current-handling terminal, and an input-transistor control terminal; and
   d. an inductor having a first inductor terminal connected to the load-control terminal and a second inductor terminal connected to the second load terminal.

2. The amplifier of claim 1, further comprising a second inductor connected between the second inductor terminal and the second load terminal.

3. The amplifier of claim 2, further comprising a resistor connected between the power terminal and the second inductor terminal.

4. The amplifier of claim 1, wherein the first current-handling terminal of the input transistor connects to the second load terminal via a resistor.

5. The amplifier of claim 1, wherein the first current-handling terminal of the input transistor connects to the second load terminal via a calibrated resistance, the calibrated resistance comprising a third transistor having a third current-handling terminal connected to the first current-handling terminal of the input transistor, a fourth current-handling terminal connected to the second load terminal, and a resistance-control

terminal.

6. The amplifier of claim 5, further comprising a calibration circuit adapted to provide a control voltage on a calibration-circuit output terminal connected to the resistance-control terminal.

7. The amplifier of claim 6, wherein the calibration circuit comprises:
   a. a reference resistor adapted to conduct a reference current;
   b. a fourth transistor adapted to conducts a second current and having a first current-handling terminal, a second current-handling terminal, and a control terminal; and
   c. a differential amplifier having:
      i. a first differential input terminal adapted to receive a first input signal of a first magnitude proportional to the reference current;
      ii. a second differential input terminal adapted to receive a second input signal of a second magnitude proportional to the second current; and
      iii. a differential-amplifier output terminal connected to the resistance-control terminal.

8. The amplifier of claim 7, wherein the differential-amplifier output terminal connects to the control terminal of the fourth transistor.

9. An amplifier comprising:
   a. first and second power-supply terminals;
   b. a current source having a current-source input terminal and a current-source output terminal connected to the first power-supply terminal;
   c. a first input transistor having a first current-

handling terminal connected to the current-source input terminal, a second current-handling terminal, and a first control terminal;

d. a second input transistor having a third current-handling terminal connected to the current-source input terminal, a fourth current-handling terminal, and a second control terminal;

e. a first resistor having first and second resistor terminals, the first resistor terminal connected to the second current-handling terminal;

f. a second resistor having third and fourth resistor terminals, the third resistor terminal connected to the fourth current-handling terminal;

g. a first load transistor having a first load terminal connected to the second power-supply terminal, a second load terminal connected to the second resistor terminal, and a first load-control terminal connected to the fourth resistor terminal;

h. a second load transistor having a third load terminal connected to the second power-supply terminal, a fourth load terminal connected to the fourth resistor terminal, and a second load-control terminal connected to the second resistor terminal;

i. a third resistor having a fifth resistor terminal connected to the second power-supply terminal and a sixth resistor terminal;

j. a first inductor connected between the second and sixth resistor terminals; and

k. a second inductor connected between the fourth and sixth resistor terminals.

10. The amplifier of claim 9, further comprising a differential output stage having a first differential input terminal connected to the second current-handling terminal and a second differential input terminal connected to the fourth current-handling terminal.

11. The amplifier of claim 9, wherein the transistors are MOS transistors.

12. The amplifier of claim 11, wherein the load transistors are PMOS transistors.

13. The amplifier of claim 9, wherein the third resistor is of a value selected so the first and second load transistors operate in saturation.

14. The amplifier of claim 9, wherein the geometries of the load transistors and inductors are selected to provide a resonant frequency of about 5GHz.

15. The amplifier of claim 1, wherein the inductor comprises a coil.

16. An amplifier load comprising:
    a. a first load transistor having a first current-handling terminal connected to a power terminal, a second current-handling terminal, and a first control terminal;
    b. a second load transistor having a third current-handling terminal connected to the power terminal, a fourth current handling terminal connected to the first control terminal, and a second control terminal connected to the second current-handling terminal; and
    c. an inductor connected between the second and fourth current-handling terminals.

17. The load of claim 16, further comprising a second inductor connected in series with the first conductor between the second and fourth current-handling terminals.

18. The load of claim 17, further comprising a bias resistor

having a first terminal connected to the power terminal and a second terminal connected between the first and second inductors.

19. The load of claim 17, wherein the first and second inductors are portions of a single center-taped inductor.

20. The load of claim 16, wherein the inductors comprises a coil.

21. The load of claim 20, wherein the coil has at least three turns.

22. The load of claim 16, wherein the first and second load transistors exhibit respective first and second gate capacitances, and wherein the inductor is of a value selected to provide a resonant frequency of about 5 GHz.

23. A circuit for calibrating a resistance between a first circuit node and a second circuit node, the circuit comprising:
    a. a reference resistor connected between first and second reference nodes;
    b. a first transistor having a first current-handling terminal connected to the first reference node, a second current-handling terminal, and a first control terminal; and
    c. a second transistor having a third current-handling terminal connected to the first circuit node, a fourth current-handling terminal connected to the second circuit node, and a second control terminal connected to the first control terminal.

24. The circuit of claim 23, further comprising a differential amplifier having a first differential input terminal connected to the second reference node, a

second differential input terminal connected to the second current-handling terminal, and a differential-amplifier output terminal connected to the first and second control terminals.

25. The circuit of claim 24, further comprising a first current source connected to the second reference node and a second current source connected to the second current-handling terminal of the first transistor.

26. The circuit of claim 25, wherein the first current source includes a third transistor having a third-transistor control terminal, the second current source includes a fourth transistor having a fourth-transistor control terminal connected to the third-transistor control terminal.

27. The circuit of claim 23, further comprising a second resistor connected between the first and second circuit nodes.

28. The circuit of claim 23, further comprising a second resistor connected between the first and second current-handling terminals of the first transistor.

29. A circuit for calibrating a resistance between a first circuit node and a second circuit node, the circuit comprising:

a. a first reference node adapted to provide a first reference voltage;

b. a second reference node adapted to provide a second reference voltage;

c. a reference resistor connected between the first and second reference nodes and adapted to conduct a reference current;

d. a first transistor having a first current-handling terminal, a second current-handling terminal, and a

first control terminal, wherein the first transistor is adapted to conduct a second current;

e. a differential amplifier having:

i. a first differential input terminal adapted to receive a first input signal of a first magnitude proportional to the reference current;

ii. a second differential input terminal adapted to receive a second input signal of a second magnitude proportional to the second current; and

iii. a differential-amplifier output terminal connected to the first control terminal; and

f. a second transistor having a third current-handling terminal connected to the first circuit node, a fourth current-handling terminal connected to the second circuit node, and a second control terminal connected to the differential-amplifier output terminal.

30. The circuit of claim 29, further comprising a second resistor connected between the first and second current-handling terminals.

31. The circuit of claim 29, further comprising a second resistor connected between the third and fourth current-handling terminals.

32. The circuit of claim 31, further comprising a third resistor connected between the first and second current-handling terminals.

33. The circuit of claim 32, wherein the second and third resistors exhibit equivalent resistances.

34. The circuit of claim 32, wherein the second and third resistors are fabricated together on an integrated

circuit, and wherein the reference resistor is external to the integrated circuit.

35. The circuit of claim 29, wherein the reference current and the second current are substantially equal.

36. The circuit of claim 29, wherein the second transistor conducts a third current of a third magnitude, and wherein the second and third magnitudes are substantially equal.

37. A circuit for calibrating a resistance between a first circuit node and a second circuit node, the circuit comprising:

a. a reference resistor connected between first and second reference nodes;

b. a current source connected to the second reference node and adapted to provide a reference current through the reference resistor;

c. a first transistor having a first current-handling terminal connected to the first reference node, a second current-handling terminal, and a first control terminal, wherein the first and second current-handling terminals are adapted to conduct a second current; and

d. a differential amplifier having:

i. a first differential input terminal adapted to receive a first input signal of a first magnitude proportional to the reference current;

ii. a second differential input terminal adapted to receive a second input signal of a second magnitude proportional to the second current; and

iii. a differential-amplifier output terminal connected to the first control terminal.

38. The circuit of claim 37, further comprising a second transistor having a third current-handling terminal connected to the first circuit node, a fourth current-handling terminal connected to the second circuit node, and a second control terminal connected to the first control terminal.

39. The circuit of claim 38, further comprising a second resistor connected between the third and fourth current-handling terminals of the second transistor.

40. The circuit of claim 37, further comprising a second resistor connected between the first and second current-handling terminals of the first transistor.

41. The circuit of claim 37, further comprising a second current source adapted to provide the second current through the first transistor.